DG508BEY Charge Injection Evaluation Board Manual

DESCRIPTION

Charge injection is quite likely one of the more critical parameters of any analog switch or multiplier (mux). Charge injection performance is one of the key specifications of the semiconductor analog switch or mux. Datasheets often include the typical charge injection curves. This information is used for estimating the voltage spike on the output of the switch. The user needs to take special note of the size of the load capacitor, C_L found in the test conditions within all data sheets.

CMOS analog switches and muxes have as their switching element an n-channel MOSFET in parallel with a p-channel MOSFET, the combination offering the classic bathtub resistance response as shown in figure 1. However, as a consequence of parasitic capacitances between Gate and channel - C_{gs} and C_{gd} - and because of the swiftness of the transitional gating voltage that actuates the MOSFETs, a charge is coupled to the channel resulting in voltage spikes on the signal, exiting the switch or mux at both its input (S) and output (D). The magnitude of these spikes is dependent on several factors: the speed (frequency) of the gate voltage pulse; and the size of the parasitic gate-to-channel capacitances, and of course the load capacitance, C_L. Although attempts have been made to calculate the magnitude of these spikes, because of the nonlinearity of C_{gs} and C_{gd}, we find that the optimum means of determining Charge Injection, Q_{INJ} is by measurement. Hence this Manual.

On all analog switch or mux data sheets we see this parameter identified as Q_{INJ}. Careful examination of the test conditions indicate that the input to the switch (terminal “S”) has R_{GEN} set to 0 Ω and V_{GEN} set to 0 V. As a result the anomalous charge injection (Q_{INJ}) is only considered at the output of the switch.

For precision data acquisition applications we may recognize a need for more precision in our understanding of Q_{INJ} of our particular analog switch or mux. The bench evaluation of charge injection for the DG508BEY described in this manual identifies the test methods and results. To ease the procedure the tests are conducted with this specially - designed board when the channel is on and off where we are able to quantified Q_{INJ}.

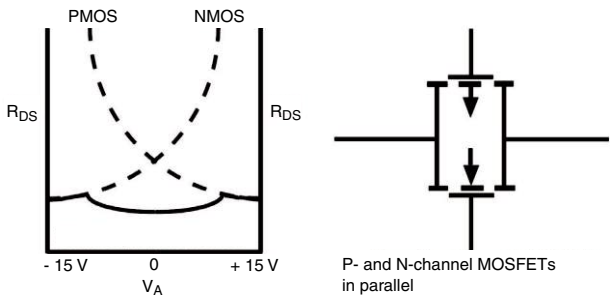


Figure 1.

TEST METHOD

Although we have been forewarned that the test conditions for charge injection demand that the input to the analog switch or mux is essentially a short-circuit (R_{GEN} = 0) it is important to recognize that for all analog switch or mux products performance is equal in both directions. One can input into either S or D. The CMOS is symmetrical. Consequently, for ease in analysis we evaluate Q_{INJ} at the input or S terminals recognizing that what we measure there duplicates what appears at D.

The schematic diagram of figure 2 identifies the circuit configuration for channel S8 injection voltage.

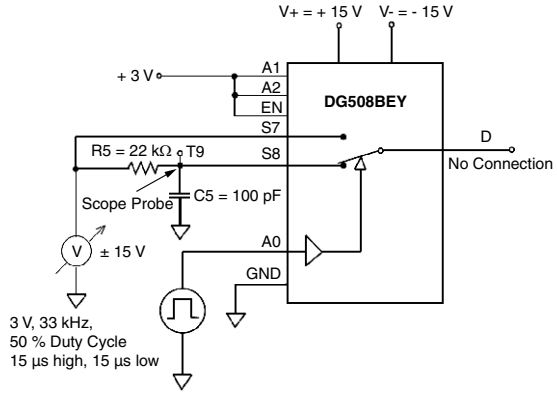


Figure 2.

In all cases the bias voltage for S7 should be set to the required value within the range of + 15 V to - 15 V, and S8 should be connected through a 22 kΩ resistor (R5) to the same bias voltage (V_{bias}). Additionally a 100 pF capacitor (C5) should be connected between S8 and ground. The output of the analog switch or mux is left floating.

The voltage resulting from charge injection is measured using an AC-coupled probe (11 pF || 10 MΩ) connected to S8 (at T9 of figure 2). Set the oscilloscope for 100 mV/div and 5 µs/div.

A function generator connects to A0 is used for toggling the address line A0 which will toggle S7 and S8.

Power Supply Terminals

For this examination of charge injection the DG508BEY is powered from ± 15 V. Terminal J3 (see figure 4) is the ground connection. Terminal J4 is the + 15 V power connection and Terminal J2 is the connection to - 15 V. Terminal J1 is used for powering the logic control and should be connected to a (+ 3 V typical) power supply.

Logic Control

There are four jumpers to control the enable function (EN) and logic (A#). The jumpers are designated as P1 for EN, P2 for A0, P3 for A1 and P4 for A2. Refer to the truth table (table 1) for the proper logic.

TABLE 1				
A2	**A1**	**A0**	**EN**	**On Switch**
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Figure 3 identifies the jumper positions for setting each control bit to 0 logic or 1 logic.

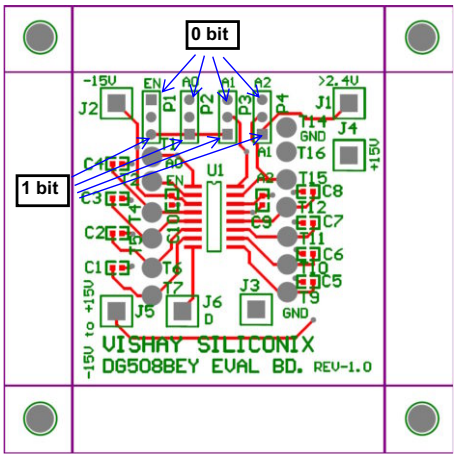


Figure 3.

V_{bias} Voltage

Continuing with figure 4 Terminal J5 is the connection for the biasing voltage. The biasing voltage ranges from - 15 V to + 15 V.

Test Point

Although this evaluation board is designed to evaluate the charge injection at all channel combinations, the schematic (figure 2) is offered as an example for testing S8 and S7.

There are a total of eight test points available to measure each switch channel. These are: T4 for S1, T5 for S2, T6 for S3, T7 for S4, T9 for S8, T10 for S7, T11 for S6, and T12 for S5.

Toggling Access Point

In addition to the logic control setting jumpers there are four toggling connections for A0, A1, A2 and EN. T1 for A0, T2 for EN, T16 for A1, and T15 for A2. The function generator can be connected to these connections to turn on and off the selected channels of the analog switch.

RC Network Configuration

The DG508BEY evaluation board is designed to configure all the testing channel combinations. The RC component can be populated on the board-as we see in figure 4 to evaluate any channel combination.

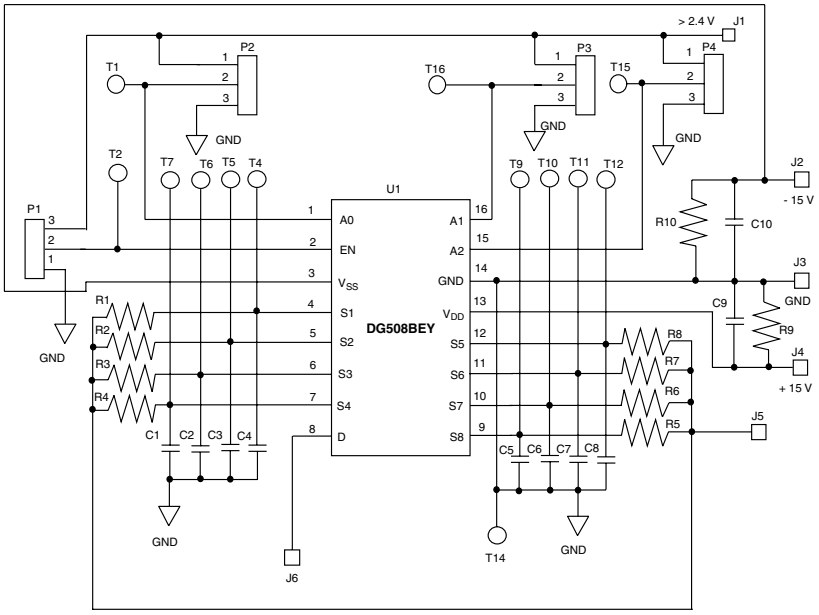
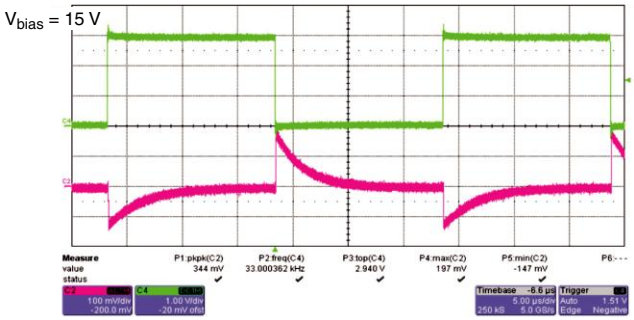


Figure 4.

TEST SETUP CONNECTION

Figure 5 shows the setup connection for measuring charge injection for S8. The resulting voltage waveform is measured at terminal T9. The toggling is applied to Terminal T1, which is the A0 pin.

The measured waveforms for A0 and S8 are shown in figure 6.



S8 on and S7 off (rising edge): - 147 mV
S8 off and S7 on (falling edge): + 197 mV

Figure 6.

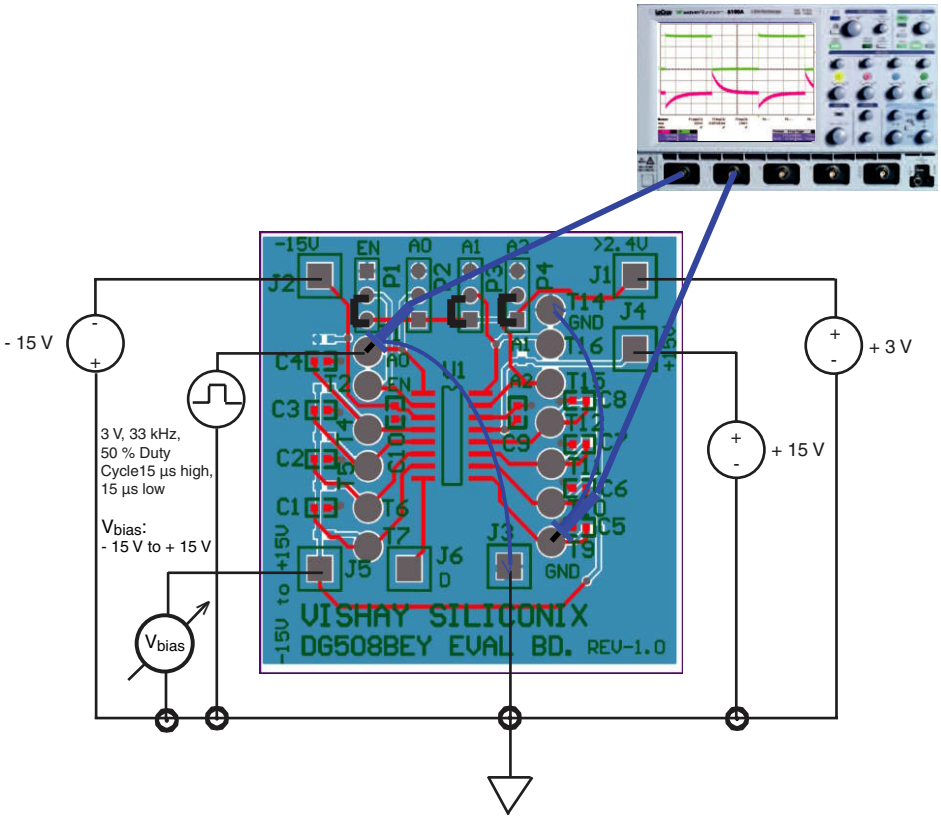


Figure 5.

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